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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/630,883	08/02/2000	Khosrow Golshan	82259/156	7954

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EXAMINER

CHANG, AUDREY Y

ART UNIT	PAPER NUMBER
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2872

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/630,883	Applicant(s) GOLSHAN, KHOSROW	
	Examiner Audrey Y. Chang	Art Unit 2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 23-30 and 47-78 is/are pending in the application.
- 4a) Of the above claim(s) 23-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 47-78 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 June 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Remark

- This Office Action is in response to applicant's amendment filed on **June 20, 2006**, which has been entered into the file.
- By this amendment the applicant has amended claims 68 and 77.
- **Claims 23-30 are withdrawn** from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.
- Claims 47-78 remain pending in this application.
- The rejections of claims 68 and 77 under 35 U.S.C. 112, first paragraph, set forth in the previous Office Action are withdrawn in response to applicant's amendment.

Drawings

1. The drawings were received on June 20, 2006. These drawings are not accepted.
2. The **drawings (filed on June 20, 2006) are objected to as failing** to comply with 37 CFR 1.84(p)(4) because reference characters "720" and "705" have both been used to designate the same element in Figure 8. No explicitly distinction is presented in the Figure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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The applicant is respectfully noted that even though the characters may be explained in the specification to refer to different elements, the drawings are still required to make the distinction between the two. Figure 8 still shows that the same element being designated by both characters “705” and “720”.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 55-64 are rejected under 35 U.S.C. 112, first paragraph**, as containing subject matter which was not described in the specification in such a way as to **enable** one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 55 has been amended to include the phrase “a predetermined axis in the interference region along which maximum interference of optical signals in the interference region is caused”.

The specification and claims fail to teach how could the maximum interference be **caused** “along a predetermined *axis* in the interference region”. The applicant is respectfully requested to study the standard optic textbook for “interference”. It is not clear how could the interference be caused along an axis. It is possible to define a direction along such the constructive interference occurs.

Claims 56-64 inherit the rejection from their based claim.

The applicant is respectfully reminded that even though the maximum interference may occur along an axis in the interference region, the axis DOES NOT cause the interference and DOES NOT cause the maximum interference.

Claim Objections

5. Claims 47-78 are objected to because of the following informalities:

(1). The newly amended phrase “the periphery being a single, outer periphery” recited in the amended claims 47, 55, 65 and 69 is confusing and indefinite for it is not clear what does this “single” mean? Judging from Figure 8, each of the interference regions has outer periphery made up of two parts, (element 760 and element 705). How do these two elements being considered as single periphery?

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 47-58, and 63-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al (PN. 5,233,205).**

Usagawa et al teaches an *optical logic circuit* based on quantum well design wherein the optical logic circuit comprises a *substrate* comprising a *first optical material*, (such as 50 in Figure 5A or 95 in Figure 6A or 6B), and a *second optical layer overlaying the substrate* wherein the second optical layer are formed or patterned to have a plurality of *optical pathways* or *optical conduits*, (52 in Figure 5A or 100, 101 and 102 in Figure 6B), wherein an *interference regions* are formed of the second optical layer as shown in Figures 1A to 1G. Usagawa et al teaches that a plurality of *waveguides* (3, 4, and 5) are used to provide *optical input signals* to a plurality of *input gates* (10, 10' and 10''), wherein the optical input signals *enter* and *intercepts* at a three-dimensional region surrounded and *defined* by potential barriers (1),

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which then serves as the *interference region*, that includes or is connected to at least one *output window* (300') such that the input optical signals intercept and interfere with each other. An *output gate* (20, Figures 1A to 1G) is connected with the interference region to provide an *optical output signal*. Usagawa et al teaches that the optical output signal is a *Boolean logic output signal*, wherein the optical logic circuit can be designed to provide NOT (invert, Figure 1D), NOT AND (NAND, Figure 1F), and exclusive OR (NOR Figure 1G) optical logic functions, respectively.

Claims 47, 55, 65 and 69 have been amended

With regard to the feature concerning the interference region comprises the second materials and is bounded on its periphery by material other than the second material and the periphery being a single, outer periphery such that only the interference region is within the periphery, as recited in **claims 47, 55, 65 and 69**, this feature is not clearly supported by the specification and is objected for the reasons stated above. Usagawa et al teaches explicitly that the interference region is the region defined by the optical pathways or conduits (52, or 101-109), that optical signals pass through and interfere with each other. Usagawa et al teaches *explicitly* that the optical pathways or optical conduits or the interference region comprises the second material such as GaAs and the interference region is bounded at its periphery (such as barrier 2, 2' and 1 in Figures 1A-3E and 51 in Figure 5A, please see columns 5 and 11) by a material such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$, which is different from the GaAs material for making up the interference region. As shown in Figure 5A of Usagawa et al the periphery that surrounds the interference region (52) is a **single outer periphery** the same way as the instant application shows in Figure 8. With regard to the amended claim 65, the second material GaAs is optical transmission material.

With regard to the feature that the "output signal having one of two intensities, either a substantially on or a substantially off intensity". This feature is implicitly met by the disclosure of Usagawa et al, since Usagawa et al teaches a *Boolean logic gate* and the optical output signal is a *Boolean logic output signal*, which implicitly include ON and OFF output intensities.

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With regard to claims 48, 51, 56-58, 66, 70-72, and 74, Usagawa et al teaches the optical logic circuit may be designed to give NOT logic function as the output signal, (Figure 1D), wherein an optical input signal may be a *constant coherent input signal*, (“1”) that enters the interference regions through the input gate (10), and a *second input coherent optical signal* (X) may be switched ON or OFF and enters the interference region through the *second input gate* (10’). When the second coherent input signal is turned ON, the input signals from both gates interfere with each other to essentially cancel each other so that an invert or NOT optical logical function is resulted as the optical output signal, (please see Figure 1D, column 8, lines 8-25).

With regard to claims 49-50, 67, 68, 69, 75, and 77, Usagawa et al teaches that the optical logic circuit may be designed to give NAND logic function, (Figure 1F), wherein three input optical signals are used. One skilled in the art certainly can design the optical processor to comprise various logic gates for the desired logical functions and purposes.

This reference has met all the limitations of the claims. With regard to the feature concerning “*the output is positioned along a chosen line, of many lines, along which destructive interference occurs*”. Usagawa et al does not teach such explicitly however this feature is to the least inherently met by the cited reference **since** the optical logic gate of Usagawa et al *performs the same Boolean logic functions* as the instant application and the output signal of the Boolean logic function is the *direct result of the interference* of the input optical signals, the arrangement of the output therefore has to align in the claimed manner to produce the Boolean logic output results. With regard to the feature of the “*interference line is aligned with the output when the light input at the second input is on*”. This feature is implicitly included in the disclosure since only when light propagates through the pathways, the quantum waves are generated. It is implicitly true that within the interference region there is at least one axis along which maximum constructive interference would occur.

With regard to claim 69, it is implicitly true that the interference properties of the input signals in the interference region are determined by the input signals and the physical structure of the interference region.

With regard to claims 63 and 64, this reference also does not teach explicitly that a laser diode or a semiconductor diode is used as the light source for generating the optical wave. However laser diode or laser semi-conductive diode are both well known light sources for operating optical logic circuit, such feature is either inherently met or an obvious modification to one skilled in the art for providing proper light sources with proper energy required to operate the optical logic circuit.

8. Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al as applied to claim 55 above, and further in view of the patent issued to Logan et al (PN. 3,837,728).

The optical logic circuit taught by Usagawa et al as described for claim 55 above has met all the limitations of the claims. Usagawa et al teaches that the optical logic circuit may use gallium arsenide (GaAs) material as the substrate layer however it does not teach explicitly to use doped GaAs material, silicon or doped silicon materials as the substrate layer and optical layer for pathways (i.e. waveguides) respectively. However these materials are all well known semi-conductive materials for making waveguides or even optical logic circuit, as demonstrated by the teachings of Logan et al wherein a GaAs layer is used as substrate layer wherein doped GaAs layer is used as the optical waveguide. It would then have been obvious matters of design choices to one skilled in the art to use the claimed materials as the materials for designing the optical logic circuits for the benefit of using desired materials that provide the desired performance. It has also been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Response to Arguments

9. Applicant's arguments filed on June 20, 2006 have been fully considered but they are not persuasive.

10. In response to applicant's arguments which state that the cited Usagawa reference does not teach "the interference region comprises the second material and is bounded on its periphery by material other than the second material, the periphery being a single outer periphery such that only the interference region is within the periphery", the examiner respectfully disagrees for the reasons stated below. The applicant has correctly identified that the interference region (52) of Usagawa which comprises second material of GaAs, is *surrounded* by the $\text{Al}_x\text{Ga}_{1-x}\text{As}$, 50 and 51 as shown in Figure 5a of Usagawa. The element (50) in Figure 5a of Usagawa serves as the **substrate** the same way as the element (705) of Figure 8 of the instant application serves as the substrate, and the interference region (52) of Usagawa is identical with the interference region (710) of Figure 8 of the instant application. The interference region (52) is surrounded by a material (51) $\text{Al}_x\text{Ga}_{1-x}\text{As}$ other than the material of the interference region (52) (i.e. GaAs) and the periphery being a *single outer periphery* such that only the interference region is within the periphery, the same as the material (760) showing in Figure 8 of the instant application. Figure 5a of Usagawa therefore shows explicitly the **same structure** as Figure 8 of the instant application wherein the interference region (52 of Usagawa same as 710 of instant application) is surrounded by the substrate (50 of Usagawa same as 705 of instant application) and the other material (51 of Usagawa same as 706 of instant application) forming an outer periphery.

11. In response to applicant's arguments which state that the cited Usagawa et al although teaches wave-like behavior of electron waves, light is not propagated through the material cause destructive interference, the examiner respectfully disagrees for destructive and constructive interferences are natural wave phenomenon for wave-like behavior.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

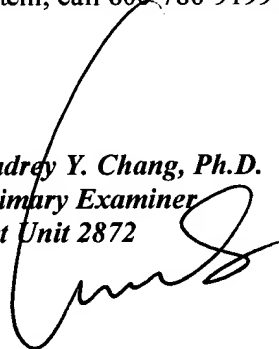
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 571-272-2309. The examiner can normally be reached on Monday-Friday (8:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Dunn can be reached on 571-272-2312. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Audrey Y. Chang, Ph.D.
Primary Examiner
Art Unit 2872



A. Chang, Ph.D.